SYLLABUS

DR VISHWANATH KARAD

MIT - WORLD PEACE UNIVERSITY

FACULTY OF ENGINEERING AND TECHNOLOGY

M.TECH. (ELECTRONICS AND COMMUNICATION ENGINEERING – VLSI AND EMBEDDED SYSTEMS)

PROGRAMME STRUCTURE

Preamble:

The School of Electronics and Communication Engineering offers very focused and specialized masters programs (M. Tech.). One of the important objectives of this program is to create Industry ready professionals to work and research in the emerging areas of electronics, information and communication technologies.

This Two Year Full-time Masters programs comprises of core courses, electives, seminars, peace related courses and a dissertation along with the internship. The students are offered wide variety of electives so that they become industry ready and get specialized in the areas of their choice.

The M. Tech. students are also involved as Teaching Assistants for teaching undergraduate students and for research. While studying theory courses, the students undergo laboratory practice for the courses they have studied. In addition to regular electives taught in the classes, along with M. Tech. dissertation, the students choose open electives of their choice to sharpen their skills. The students can either take up full-time research project or Industry project or combination of these for two trimesters.

M. Tech. Research laboratories are equipped with the state-of-the-art infrastructure including efficient computing platforms, advanced hardware boards and equipment, various licensed and open source software tools required for research purpose. They have to publish at least one research paper prior to submitting M. Tech. dissertation. Currently, the School offers two years full-time masters programs in:

- M. Tech. in Electronics and Communication Engineering with specialization in VLSI and Embedded Systems
- M. Tech. in Electronics and Communication Engineering with specialization in Communication Networks and Software

Dr. Arti Khaparde
Professor and Head, School of Electronics and Communication Engineering
MIT World Peace University, Pune-38

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Vision and Mission of the Programme

VISION

To be recognized as a leader in Electronics and Communication Engineering education with a strong emphasis on social and professional values

MISSION

To produce quality Electronics and Communication Engineering graduates by providing them education with applied approach, professional values through creative learning environment

Programme Educational Objectives

The Electronics and Communication Engineering Graduate will:

- Be widely employed across a range of disciplines and sub-disciplines in electronics and communication engineering.
- Have ability to tackle interdisciplinary engineering problems.
- Have quest for excellence, leadership qualities, self-discipline and lifelong learning.
- Contribute for the betterment of the profession and society.

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Programme Outcomes (POs)

Electronics and Communication Engineering Graduates will be able to:

PO1 **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2 **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3 **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4 **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5 **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6 **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7 **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8 **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9 **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10 **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11 **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12 **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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Programme Specific Outcomes (PSOs)

Engineering Graduates will be able to:

PSO1 Design variety of modules and systems for applications that includes analog and digital signal processing, communication, and networks

PSO2 Utilize modern modeling and computational techniques, and tools for analyzing and solving problems associated with electronics and communication

PSO3 Demonstrate skills for handling, operating, and using various test and measurement equipment used in electronics and communication

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Programme Structure:

(a) Programme duration : Two Years

(b) System followed : Trimester

(c) Credits System:

The outcome based education, trimester based credit and grading system is introduced to ensure quality of engineering education. Trimester based credit and grading system enables a much-required shift in focus from teacher centric to learner-centric education since the workload estimated is based on the investment of time in learning and not in teaching. It also focuses on continuous evaluation which will enhance the quality of education.

(i) Per term or per year : Credits are given per trimester
(ii) Total in the programme : 66 Credits

(d) Credits for activities other than academics:

In the curriculum, some credits are given to other activities such as social internship, domestic and international study tours, and Industry internship/project.

(e) Internship:

The program has rural immersion module as a part of social internship in the first year of study. The student would also have to undergo one full trimester Internship in Industry along with their project work during the final year. These credit based internships are mandatory for all the students.

(f) Assessment Criteria:

There will be continuous as well as end trimester assessment of a student's performance and grades will be awarded by the Subject Teacher. The assessment and evaluation guidelines are as below:

Component	Weight
Laboratory Continuous Assessment	25%
Class Continuous Assessment	25%
End-Semester Examination	50%

Various assessment tools such as tests, quizzes, assignments, project, group activities, presentations, etc would be used to evaluate the performance of the students.

(g) Mandatory Attendance to appear for examination: 90%

As per Para 13.1, Academic Ordinance: 2017 of MIT-WPU, It is expected on the part of the student to attend each and every Lecture, Tutorial, and Laboratory practical sessions in a course for the academic excellence. However, due to any contingencies, the attendance requirement will be a minimum of 90% of the classes scheduled/ held.

(h) Medium of Instruction & Examination: *English*

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As per Para 9, Academic Ordinance: 2017 of MIT-WPU, in all the Academic Programs, the medium of instruction and examination shall be English.

(i) Eligibility criteria for admission to the programme:

As per Para 4, Academic Ordinance: 2017 of MIT-WPU, the eligibility criteria for First Year admission is as below:

1. **UG Eligibility (BE/BTech):**
   Computer Science and Engineering, Computer Engineering, Computer Technology, Computer Science and Technology, Electronics and Communication Engineering, Electronics and Telecommunication Engg, Electronics Engineering, Electronic and Communication Technology, Instrumentation and Control Engineering, Instrumentation Engineering, Industrial Electronics or equivalent

2. **GATE Eligibility:**
   Computer Science and Information Technology (CS), Electronics and Communication Engineering (EC), Instrumentation Engineering (IN)

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M. Tech Courses in Electronics and Communication Engineering
VLSI and Embedded Systems

2018-19

A. Definition of Credit:

3 Hours. Lecture / Tutorial per week	2 Credits
2 Hours Practical (Lab) per week	1 Credit

B. Credits:

Total number of credits for two year M.Tech. Electronics and Communication Engineering – VLSI and Embedded Systems Programme would be 175.

C. Structure of Credits for Undergraduate M.Tech. Electronics and Communication Engineering – VLSI and Embedded Systems:

S. No.	Category	Suggested Breakup of Credits (Total 66)
1	Humanities and Social Sciences and Peace Programmes including Management courses	8
2	Engineering Science courses	2
4	Professional core courses	24
5	Professional Elective courses relevant to chosen specialization/branch	8
6	Open subjects–Electives from other technical and/or emerging subjects	2
7	Project work, seminar and internship in industry or elsewhere	22
	Total	**66**

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D. *Course Code and Definition:*

Course code	*Definitions*
L	Lecture
T	Tutorial
WPP	Humanities and Social Sciences and Peace Programs including Management courses
ECV	Electronics and Communication (VLSI and Embedded Systems)

E. Grading Scheme:

According to Para 12.1 of Academic Ordinances 2017, University shall use trimester /semester / annual as per need of a program. The credit based system provides flexibility in designing curriculum and assigning credits based on the course content and hours of teaching. The choice based credit system provides a 'cafeteria' type approach in which the students can take courses of their choice, learn at their own pace, undergo additional courses and acquire more than the required credits, and adopt an interdisciplinary approach to learning. The University shall follow a 10-point grading system with the following letter grades as given below:

Marks Out of 100	**Grade**	**Grade Point**
80-100	O: Outstanding	10
70-79	A+: Excellent	9
60-69	A: Very Good	8
55-59	B+: Good	7
50-54	B: Above Average	6
45-49	C: Average	5
40-44	Pass	4
0-39	Fail	0
Ab	Absent	NA

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M. Tech. Electronics and Communication Engineering – VLSI and Embedded Systems
(First Year) (Batch 2018-19)
Trimester – I

Sr. No.	Course Code	Name of Course	Type	Weekly Workload, Hrs.			Credits		Assessment, Marks			
				Theory	Tutorial	Lab.	Th.	Lab.	CCA*	LCA*	End Term Test	Total
1	ECV511	Research Methodology	Engg. Science	3	-	-	2	-	50	-	50	100
2	ECV512	Analog & Digital VLSI Design	Core	3	-	-	2	-	50	-	50	100
3	ECV513	Embedded System Design	Core	3	-	-	2	-	50	-	50	100
4	ECV514	Lab Practice-I	Core	-	-	6	-	3	-	50	50	100
5	WPC1	World Famous Philosophers, Sages/Saints and Great Kings	WPC	3	-	-	2	-	70	--	30	100
6	WPC3	Yoga – For Winning Personality	WPC	-	-	-	-	-	-	-	-	-
Total :				**12**		**6**	**8**	**3**	**220**	**50**	**230**	**500**

****Assessment Marks are valid only if Attendance criteria are met**

Weekly Teaching Hours: 18 Hours

Total Credits: First Year M. Tech ECE - VES Trimester - I: 11

***** CCA: Class Continuous Assessment

***** LCA: Laboratory Continuous Assessment

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Trimester – II

Sr. No.	Course Code	Name of Course	Type	Weekly Workload, Hrs.			Credits		Assessment, Marks			
				Theory	Tutorial	Lab.	Th.	Lab.	CCA*	LCA*	End Term Test	Total
1	ECV521	Advanced VLSI Design	Core	3	-	-	2	-	50	-	50	100
2	ECV522	Embedded Signal Processing	Core	3	-	-	2	-	50	-	50	100
3	ECV523	Elective-I	Departmental Elective	3	-	-	2	-	50	-	50	100
4	ECV524	Lab Practice-II	Core	-	-	6	-	3	-	50	50	100
5	WPC4	Philosophy of Science and Religion/ Spirituality	WPC	3	-	-	2	-	70	-	30	100
6	WPC3	Yoga – For Winning Personality	WPC	-	-	-	-	-	-	-	-	-
Total :				**12**	**-**	**6**	**8**	**3**	**220**	**50**	**230**	**500**

Weekly Teaching Hours: 18 Hours

Total Credits: First Year M. Tech ECE - VES Trimester - II: 11

****Assessment Marks are valid only if Attendance criteria are met**

* CCA: Class Continuous Assessment

* LCA: Laboratory Continuous Assessment

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Trimester – III

Sr. No.	Course Code	Name of Course	Type	Weekly Workload, Hrs.			Credits		Assessment Marks**			
				Theory	Tutorial	Lab.	Th.	Lab.	CCA*	LCA*	End Term Test	Total
1	ECV531	System on Chip	Core	3	-	-	2	-	50	-	50	100
2	ECV532	Elective-II	Departmental Elective	3	-	-	2	-	50	-	50	100
3	ECV533	Elective-III	Departmental Elective	3	-	-	2	-	50	-	50	100
4	ECV534	Lab Practice-III	Core	-	-	6	-	3	-	50	50	100
5	ECV535	Seminar-I	Inter-disciplinary	-	-	4	-	2	-	50	50	100
6	WPC2	Study of Languages, Peace in Communications and Human Dynamics	WPC	3	-	-	2	-	70	-	30	100
7	WPC3	Yoga – For Winning Personality	WPC	-	-	-	-	-	-	-	-	-
Total :				**12**	**-**	**10**	**8**	**5**	**220**	**100**	**280**	**600**

Weekly Teaching Hours: 22 Hours

Total Credits: First Year M. Tech ECE - VES Trimester - III: 13

Total First Year M. Tech Credits: 11+11+13= 35

****Assessment Marks are valid only if Attendance criteria are met**

* CCA: Class Continuous Assessment

* LCA: Laboratory Continuous Assessment

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M. Tech. Electronics and Communication Engineering - VLSI and Embedded Systems (Second Year) (Batch 2018-19)

Trimester – IV

Sr. No.	Course Code	Name of Course	Type	Weekly Workload, Hrs.			Credits		Assessment Marks**			
				Theory	Tutorial	Lab.	Th.	Lab.	CCA*	LCA*	End Term Test	Total
1	ECV611	Testing & Testability	Core	3	-	-	2	-	50	-	50	100
2	ECC612	Artificial Intelligence Techniques and Applications	Core	3	-	-	2	-	50	-	50	100
3	ECV613	Elective-IV	Inter-disciplinary/ Skill	3	-	-	2	-	50	-	50	100
4	ECV614	Project Stage -I Seminar	Core	-	-	4	-	2	-	50	50	100
5	ECV615	Lab Practice-IV	Core	-	-	6	-	3	-	50	50	100
6	WPC3	Yoga – For Winning Personality	WPC	-	-	-	-	-	-	-	-	-
Total :				9	-	10	6	5	150	100	250	500

Weekly Teaching Hours: 19 Hours

Total Credits Second Year M. Tech ECE – VES Trimester - I: 11

****Assessment Marks are valid only if Attendance criteria are met**

* CCA: Class Continuous Assessment

* LCA: Laboratory Continuous Assessment

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Trimester – V

Sr. No.	Course Code	Name of Course	Type	Weekly Workload, Hrs.			Credits		Assessment Marks**			
				Theory	Tutorial	Lab.	Th.	Lab.	CCA*	LCA*	End Term Test	Total
1	ECV621	Elective-V	Web-based Open Source	2	-	-	1	-	-	-	50	50
2	ECV622	Project Stage -II Seminar	Core	-	-	18	-	9	-	100	50	150
3	WPC3	Yoga – For Winning Personality	WPC	-	-	-	-	-	-	-	-	-
Total :				2	-	18	1	9	-	100	100	200

Weekly Teaching Hours: 20 Hours

Total Credits: Second Year M. Tech ECE – VES Trimester - II: 10

****Assessment Marks are valid only if Attendance criteria are met**

* CCA: Class Continuous Assessment

* LCA: Laboratory Continuous Assessment

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M. Tech. Electronics and Communication Engineering - VLSI and Embedded Systems (Second Year) (Batch 2018-19)

Trimester – VI

Sr. No.	Course Code	Name of Course	Type	Weekly Workload, Hrs.			Credits		Assessment Marks**			
				Theory	Tutorial	Lab.	Th.	Lab.	CCA*	LCA*	End Term Test	Total
1	ECV631	Elective-VI	Web-based Open Source	2	-	-	1	-	-	-	50	50
2	ECV632	Project Stage -III Seminar	Core	-	-	18	-	9	-	100	100	200
3	WPC3	Yoga – For Winning Personality	WPC	-	-	-	-	-	-	-	-	-
Total :				2	-	18	1	9	-	100	150	250

****Assessment Marks are valid only if Attendance criteria are met**

Weekly Teaching Hours: 20 Hours

Total Credits: Second Year M. Tech ECE – VES Trimester - III: 10

***** CCA: Class Continuous Assessment

***** LCA: Laboratory Continuous Assessment

Total Second Year M. Tech Credits: 11+10+10= 31

Total M. Tech Credits: 66 Credits

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Elective Courses:

Elective-I (First Year-II) (ECV523)	Elective-II (First Year-III) (ECV532)	Elective-III (First Year-III) (ECV533)	Elective-IV (Second Year-IV) (ECV613)	Elective-V (Second Year-V) (ECV621)	Elective-VI (Second Year-VI) (ECV631)
a. ANN & Fuzzy Systems (ECV523A)	**a.** Mixed Signal CMOS Design (ECV532A)	**a.** Image Processing & Computer Vision (ECV533A)	**a.** Economics for Engineers (ECV613A)	Web Based (ECV621)	Web Based (ECV631)
b. Speech Processing (ECV523B)	**b.** Wireless Sensor Network (ECV532B)	**b.** CUDA Architecture & Programming (ECV533B)	**b.** Automotive Embedded System (ECV613B)		

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COURSE STRUCTURE

Course Code	**ECV511**			
Course Category	**Engg. Science**			
Course Title	**Research Methodology**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites:

1. Statistical techniques
2. Probability Theory
3. Communication Skills

Course Objectives:

1. Knowledge: To give an insight into research Process.

2. Skills: **(i)** To acquaint students with identifying problems for research and develop Research strategies.

(ii) To familiarize students with the techniques of data collection, analysis of data and interpretation

3. Attitude: To provide an idea about technical report writing and ethics.

Course Outcomes:

After completion of this course students will be able to

1. Prepare a research proposal for projects in their area of interest.
2. Accurately collect, analyze, interpret and report data.
3. Review and analyze research findings.
4. Understand ethical issues and instill confidence and professional pride in research scholars.

Course Contents:

Understanding Research Methodology

Objectives of research, Issues and problems in research, Characteristics of good research, Types, Stages in scientific research process, Experimental skills, Types of errors, Various graphical representation techniques, Study of important instruments.

Literature Review

Primary and secondary sources, Journals, Monographs-patents, Web as a source, Searching the web, Reading research paper, Reporting literature search, Identifying gap areas from literature review, Formulation of hypothesis, Writing review paper, Manuscript preparation.

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Data Collection, Analysis and Interpretation
Classification of data, Databases and indexes, Methods of data collection, Sampling, Sampling techniques procedure and methods, Data analysis, Statistical techniques and choosing an appropriate statistical technique, Data processing and presentation software, Statistical inference, Interpretation of results.

Technical Writing and Reporting of Research
Efficient communication, oral communication, written communication, presentation skills, Referencing and referencing styles for research journal, Documentation and presentation tools, Indexing and citation of journals, Research proposal preparation, Budgeting, Presentation, Funding agencies for engineering research, Intellectual property (IPR), Plagiarism, Ethical considerations in research.

Learning Resources:

Reference Books:

1. Kumar Ranjit, "Research Methodology-A Step-by-Step Guide for Beginners,"2nd Edition, Singapore, Pearson Education, 2005
2. Garg, B.L, Karadia, R., Agarwal, F. and Agarwal, "An introduction to Research Methodology," RBSA Publishers. 2002.
3. R. Ganeshan, "Research Methodology: For Engineers," MJP Publishers, 2011.
4. Kothari, C.R., "Research Methodology: Methods and Techniques," New Age International, 1990.

Supplementary Reading:

1. David V. Thiel, " Research Methods for Engineers", 1st Edition Cambridge University Press

Web Resources:

Weblinks:

1. https://www.slideshare.net/mssridhar/introduction-to-research-methodology-presentation
2. https://www.youtube.com/watch?v=TGlGn1HRDAM

MOOCs:

1. Methodology for design research
   http://nptel.ac.in/courses/107108011/
2. Introduction to Research
   http://nptel.ac.in/courses/121106007/

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Pedagogy:

1. Power Point Presentation
2. Videos
3. Group Discussion
4. Group Proposals

Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

Term End Examination: 50 Marks (100 %)

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	*Lab*	*Assess*
1	**Understanding Research Methodology:** Objectives of research, Issues and problems in research, Characteristics of good research, Types, Stages in scientific research process, Experimental skills, Types of errors, Various graphical representation techniques, Study of important instruments.	**8**	--	--
2	**Literature Review:** Primary and secondary sources, Journals, Monographs-patents, Web as a source, Searching the web, Reading research paper, Reporting literature search, Identifying gap areas from literature review, Formulation of hypothesis, Writing review paper, Manuscript preparation.	**8**	--	--
3	**Data Collection, Analysis and Interpretation :** Classification of data, Databases and indexes, Methods of data collection, Sampling, Sampling techniques procedure and methods, Data analysis, Statistical techniques and choosing an appropriate statistical technique, Data processing and presentation software, Statistical inference, Interpretation of results.	**8**	--	--
4	**Technical Writing and Reporting of Research :** Efficient communication, oral communication, written communication, presentation skills, Referencing and referencing styles for research journal, Documentation and presentation tools, Indexing and citation of journals, Research proposal preparation, Budgeting, Presentation, Funding agencies for engineering research, Intellectual property (IPR), Plagiarism, Ethical considerations in research.	**8**	--	--

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COURSE STRUCTURE

Course Code	**ECV 512**			
Course Category	**Core Engineering**			
Course Title	**Analog and Digital VLSI Design**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites:
1. Digital Electronics
2. Electronics Devices and Circuits
3. Analog Integrated Circuits

Course Objectives:

At the end of this course, Learners will be able to
1. **Simulate** MOSFET models using SPICE tools. **(Knowledge)**
2. **Estimate** circuit delay using RC delay models and logical eff orts. **(Knowledge)**
3. **Describe** the steps required for fabrication of MOSFET. **(Skill)**
4. **Differentiate** Static and Dynamic Power Dissipation in CMOS circuits. **(Skill)**
5. **Discuss** various characteristics of CMOS chips such as Variability, Reliability etc**. (Attitude)**
6. **Explain** Analog CMOS sub-circuit design using MOSFET as basic component. **(Attitude)**

Course Outcomes:

At the end of this course, Learners will be able to,

1. **Find** why MOSFET is a basic component in the chip design. **(CL I)**
2. **Explain** CMOS technologies and layout design rules. **(CL II)**
3. **Apply** layout design rules to draw layout for simple logic circuits. **(CL III)**
4. **Assess** performance of CMSO logic circuit based on Speed, Power and logical efforts. **(CL V)**
5. **Design** CMOS inverter as an amplifier. **(CL VI)**

Course Contents:

MOSFET and CMOS Basic: MOSFET - Types, Structure, operation, I-V characteristics, Non-ideal I-V effects, MOS Models - Large Signal, Small Signal, Spice Simulation of MOS Circuits, MOS Switch, MOS Diode/Active Resistor, CMOS Logic, Static CMOS Inverter, DC Transfer Characteristics.

CMOS Processing and Timing Analysis: CMOS Technologies - Fabrication, Layout Design Rules, Stick diagram and Layout Design, CMOS process Enhancements, DRC, Circuit Extraction, and Manufacturing Issues. Delay definitions, Transient response, RC Delay Model, Elmore Delay Model, Linear Delay Model, Logical Effort of a Gate and Paths.

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Circuit Characterization and Performance Estimation: Dynamic power dissipation, Static power dissipation, Power Delay Product, Energy Delay Product, Low Power Architectures, Wire Geometry, Interconnect Modeling - Impact and Engineering, Variability, Reliability, Scaling.

Basics of CMOS Analog Circuit Design: Current Sinks and Sources, Current Mirrors, Circuit and Voltage references, Bandgap Reference, CMOS inverter as an amplifier.

Learning Resources:

Reference Books:

1. Neil H. E. Weste, David Money Harris, "CMOS VLSI Design A Circuit and Systems Perspective", Pearson India Fourth Edition, 2015.
2. Sung-Mo Kang, Yusuf Leblebici, Chulwoo Kim, "CMOS Digital Integrated Circuits Analysis and Design", McGraw- Hill Education, 4th Indian Edition, 2016.
3. B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw- Hill Education, 2nd Indian Edition, 2017.
4. P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, Oxford University Press 3rd Edition 2013.
5. R. Jacob Baker et al, "CMOS Circuit Design, Layout and Simulation", IEEE Press, A John Wiley & Sons, Publication, 2011.

Supplementary Reading:

Web Resources:

Web links:

1. S. Karamalkr, "Solid State Devices", [Lecture 33 to 41] Video Course offered by NPTEL retrieved from http://nptel.ac.in/courses/117106091/.
2. A.N. Chandorkar, " CMSO Analog VLSI Design", [Lecture 1 to 10 Video Course offered by NPTEL retrieved from http://nptel.ac.in/courses/117101105/

MOOCs:

1. Yannis Tsividis, "MOS Transistor", [11 Week Course on Coursera] MOOC offered by Columbia University Retrieved on July 30, 2017 from https://www.coursera.org/learn/mosfet.

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Pedagogy:

- Power Point Presentation
- Demonstration
- Video
- Interactive

Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

Term End Examination: 50 Marks (100 %)

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	Lab	Assess
1	**MOSFET and CMOS Basic:** MOSFET - Types, Structure, operation, I-V characteristics, Non-ideal I-V effects, MOS Models - Large Signal, Small Signal, Spice Simulation of MOS Circuits, MOS Switch, MOS Diode/Active Resistor, CMOS Logic, Static CMOS Inverter, DC Transfer Characteristics.	**10**	--	--
2	**CMOS Processing and Timing Analysis:** CMOS Technologies - Fabrication, Layout Design Rules, Stick diagram and Layout Design, CMOS process Enhancements, DRC, Circuit Extraction, and Manufacturing Issues. Delay definitions, Transient response, RC Delay Model, Elmore Delay Model, Linear Delay Model, Logical Effort of a Gate and Paths.	**10**	--	--
3	**Circuit Characterization and Performance Estimation:** Dynamic power dissipation, Static power dissipation, Power Delay Product, Energy Delay Product, Low Power Architectures, Wire Geometry, Interconnect Modeling - Impact and Engineering, Variability, Reliability, Scaling.	**06**	--	--
4	**Basics of CMOS Analog Circuit Design:** Current Sinks and Sources, Current Mirrors, Circuit and Voltage references, Bandgap Reference, CMOS inverter as an amplifier.	**06**	--	--

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COURSE STRUCTURE

Course Code	**ECV513**			
Course Category	**Core Engg**			
Course Title	**Embedded System Design**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites: Under graduate courses Microprocessor, Advanced / Embedded Microcontrollers

Course Objectives:

At the end of this course, students will be able to

1. To create awareness about characteristics and design concepts of embedded systems.
2. To develop skills of programming with real time operating system for embedded systems
3. To explore embedded Linux environment.
4. To impart knowledge of latest applications of embedded systems.

Course Outcomes:

After completion of this course students will be able to

1. Understand embedded system design metrics, development life cycle. (CL-II)
2. Develop programs in RTOS environment. (CL-III)
3. Demonstrate basics of embedded Linux operating system. (CL-II)
4. Design embedded system for given application. (CL-VI)

Course Contents:

Introduction to Embedded Systems: Introduction to embedded systems, Classification and characteristics of embedded system, Design process, Design metrics and optimization, Embedded system technology, Development life cycle, Introduction to development platform trends.

Real Time Systems Concepts with µCOSII: Introduction to RTOS, Multitasking, Context switch, Kernel, Scheduler and its types, µCOSII kernel structure, services: task management, time management, inter-task communication and synchronization with semaphore, mutex, mailbox, Memory requirements.

Embedded Linux: Embedded Linux development environment, Role of a boot loader, Boot loader challenges, A universal boot loader: das U-boot, porting U-boot, Device driver concepts, Linux file system.

Real Time Embedded Applications: Case study of embedded system like car cruise control, Mobile phone, Automatic chocolate vending machine.

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Learning Resources:

Reference Books:

1. Raj Kamal, "Embedded Systems – Architecture, Programming and Design," Mc Graw Hill Education Pvt. Ltd., 2nd Edition, 2008.
2. Frank Vahid and Tony Givargis, "Embedded System Design – A Unified hardware/ Software introduction," John Wiley and sons, 3rd Edition, 2006.
3. Jean J. Labrosse, "MicroC OS II, the Real-Time Kernel," CMP Books , 2nd Edition, 2002.
4. Christopher Hallinan, "Embedded Linux Primer -A Practical, Real-World Approach," Pearson India, 2nd Edition, 2011.

Supplementary Reading:

Arnold S. Berger , "Embedded Systems Design: An Introduction to Processes, Tools, and Techniques," CMP Books, 2001

Web Resources:

Weblinks:

1. Embedded System design: http://esd.cs.ucr.edu/
2. µC/OS-II: https://www.micrium.com
3. Linux Foundation: http://www.linuxfoundation.org/
4. GCC online documentation: http://gcc.gnu.org/onlinedocs/
5. Mobile phone: http://en.wikipedia.org/wiki/Mobile_phone

MOOCs:

1. https://onlinecourses.nptel.ac.in/noc17_cs05/preview
2. https://www.edx.org/course/embedded-systems-shape-world-utaustinx-ut-6-10x
3. https://www.coursera.org/learn/introduction-embedded-systems

Pedagogy:

- Power Point Presentations, Videos
- Group Activities

Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

Term End Examination: 50 Marks (100 %)

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	Lab	Assess
1	**Introduction to Embedded Systems:** Introduction to embedded systems, Classification and characteristics of embedded system, Design process, Design metrics and optimization, Embedded system technology, Development life cycle, Introduction to development platform trends.	**8**	--	--
2	**Real Time Systems Concepts with µCOSII:** Introduction to RTOS, Multitasking, Context switch, Kernel, Scheduler and its types, µCOS II kernel structure, services: task management, time management, inter-task communication and synchronization with semaphore, mutex, mailbox, Memory requirements.	**8**	--	--
3	**Embedded Linux:** Embedded Linux development environment, Role of a boot loader, Boot loader challenges, A universal boot loader: das U-boot, porting U-boot, Device driver concepts, Linux file system.	**7**	--	--
4	**Real Time Embedded Applications:** Case study of embedded system like car cruise control, Mobile phone, Automatic chocolate vending machine.	**7**	--	--

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Course Code	**ECV514**			
Course Category	**Core Engineering**			
Course Title	**Lab Practice-I**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**0**	**0**	**6**	**0+0+3**

Pre-requisites: C/C++, Matlab

Course Objectives:

1. To acquaint students with identifying problems for research and develop Research strategies.
2. To familiarize students with the techniques of data collection, analysis of data and interpretation
3. **Differentiate** Static and Dynamic Power Dissipation in CMOS circuits. **(Skill)**
4. **Explain** Analog CMOS sub-circuit design using MOSFET as basic component. **(Attitude)**
5. To develop skills of programming with real time operating system for embedded systems
6. To impart knowledge of latest applications of embedded systems

Course Outcomes:

1. Prepare a research proposal for projects in their area of interest.
2. **Assess** performance of CMOS logic circuit based on Speed, Power and logical efforts. **(CL V)**
3. **Design** CMOS inverter as an amplifier. **(CL VI)**
4. Design embedded system for given application. (CL-VI)

Course Contents:

Research Methodology

1. Plot the given data in various ways and find statistical Parameters and interpret the result.
2. Read a research paper, understand Manuscript preparation steps and write your own conclusion on it.
3. Write a review paper and find Plagiarism report.
4. Write Research proposal in the area of your interest using Documentation and presentation tools and present it.

Analog & Digital VLSI Design

1. Design and simulate using CAD tools (Tanner/ Mentor Graphics)
2. CMOS Inverter as an amplifier
3. Current Mirror Circuit
4. 2-bit counter
5. Any circuit using transmission gate

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Embedded System Design

1. Multitasking application using Semaphore or Mutex with µCOS II RTOS
2. Intertask communication using Mailbox or Queue with µCOS II RTOS
3. Demonstration of embedded Linux booting with target device- ARM9
4. Device driver implementation with embedded Linux

Learning Resources:

Pedagogy:

1. Power Point Presentations, Videos
2. Programming skill based exercises
3. Group Activities/Mini Projects

Assessment Scheme:

Laboratory Continuous Assessment (LCA)

Performance in Experiment	Result Analysis & Conclusion	Journal/Report	Attendance/ Discipline/Initiative	Total
15 (30 %)	15 (30%)	10 (20%)	10 (20%)	50 (100%)

End semester evaluation will be based on Oral examination. *50 Marks (100%)*

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Syllabus:

Expt. No.	Title of Experiment	Workload in Hrs		
		Theory	Lab	Assess
Research Methodology				
1	Plot the given data in various ways and find statistical Parameters and interpret the result.	--	**4**	--
2	Read a research paper, understand Manuscript preparation steps and write your own conclusion on it.	--	**4**	--
3	Write a review paper and find Plagiarism report.	--	**4**	--
4	Write Research proposal in the area of your interest using Documentation and presentation tools and present it.	--	**4**	--
Analog & Digital VLSI Design				
1	Design and simulate using CAD tools (Tanner/ Mentor Graphics)	--	**4**	--
2	CMOS Inverter as an amplifier	--	**4**	--
3	Current Mirror Circuit	--	**4**	--
4	2-bit counter	--	**4**	--
5	Any circuit using transmission gate	--	**4**	--
Embedded System Design				
1	Multitasking application using Semaphore or Mutex with µCOS II RTOS	--	**4**	--
2	Intertask communication using Mailbox or Queue with µCOS II RTOS	--	**4**	--
3	Demonstration of embedded Linux booting with target device- ARM9	--	**4**	--
4	Device driver implementation with embedded Linux	--	**4**	--

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COURSE STRUCTURE

Course Code	**ECV 521**			
Course Category	**Core Engineering**			
Course Title	**Advanced VLSI Design**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites: ECV512 Analog and Digital VLSI Design

Course Objectives:

At the end of this course, Learners will be able to,

1. **Describe** the architecture of CPLD and FPGA. **(Knowledge)**
2. **Develop** project based on FPGA/CPLD through HDL language **(Knowledge)**
3. **Write** Verilog codes for modelling various digital logic blocks. **(Skill)**
4. **Build** the complex logic circuit using minimal logic blocks. **(Skill)**
5. **Practice** the VLSI Digital design flow using Xilinx/Intel/Mentor EDA tools. **(Attitude)**
6. **Explain** VLSI design automation concepts. **(Attitude)**

Course Outcomes:

At the end of this course, Learners will be able to,

1. **Model** digital circuits by using Verilog HDL language. **(CL III)**
2. **Design** and optimize digital logic circuits. **(CL VI)**
3. **Outline** the architecture of PLDs developed by chip design vendors. **(CL II)**
4. **Determine** Arithmetic Implementation Strategies for VLSI. **(CL V)**
5. **Explain** VLSI Design Automation Concepts. **(CL II)**

Course Contents:

Digital Design using Verilog HDL: Importance of HDLs, Introduction to Verilog, Language elements, Lexical Conventions, Value Set, Data types, Modules and ports, Operands, Operators, Expressions, Delays, Compiler Directives, Tasks and Functions, Synthesis and Simulation, Test Benches, Gate-level Modeling, Dataflow Modeling, Behavioral Modelling, Structural Modeling, Mixed Modeling Techniques, Realization of combinational and sequential circuits using Verilog.

Programmable Logic devices and their architecture: Types of Simple programmable logic devices – ROMs, PLAs, PALs, GALs; Complex Programmable Logic Devices, FPGA programming technologies - SRAM, Anti-fuse, EPROM, EEPROM, Flash; FPGA design flow, Programmable Logic blocks, Programmable Interconnects and Programmable I/O bocks in FPGAs, Applications of FPGAs, Microsemi (formerly Actel) ACT series, Xilinx LCA series, Intel (formerly Altera) flex series, Intel Max series.

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Data Path Design: Arithmetic Implementation Strategies for VLSI, Bit Serial Arithmetic, Bit Parallel Arithmetic, full adder, Mirror adder, Carry bypass adder, Carry select adder, Carry look ahead adder.

VLSI Design Automation: Brief overview of basic VLSI Design automation concepts, netlist and system partitioning, timing analysis in the context of physical design automation, placement algorithm.

Learning Resources:

Reference Books:

1. Stephen Brown, Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design" McGraw-Hill Education Third Edition, 2014.
2. Samir Palnitkar, "Verilog HDL A guide to Digital Design and Synthesis", Prentice Hall Second Edition, 2003.
3. J. Bhaskar, "Verilog HDL Synthesis A Practical Primer", Star Galaxy Press Second Edition.
4. Wayne Wolf, "FPGA-Based System Design", Pearson India First Edition, 2009.
5. Stephen D. Brown, Robert J Francis, Jonathan Rose, Ivonko G. Vranesic, "Field Programmable Gate Arrays", Springer International Edition, First Indian Print 2007.
6. Jan M.Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, "Digital Integrated Circuits", Pearson India, Second Edition, 2016.
7. Neil H. E. Weste, David Money Harris, "CMOS VLSI Design A Circuit and Systems Perspective", Pearson India Fourth Edition, 2015.
8. Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer 2011.

Supplementary Reading:

Web Resources:

Web links:

1. www.xilinx.com
2. www.altera.com
3. www.asic-world.com

MOOCs:

1. Advanced VLSI Design: nptel.ac.in/courses/117101004/
2. https://www.coursera.org/learn/intro-fpga-design-embedded-systems

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Pedagogy:

- Power Point Presentation
- Demonstration
- Video
- Interactive

Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

Term End Examination: 50 Marks (100%)

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	Lab	Assess
1	**Digital Design using Verilog HDL:** Importance of HDLs, Introduction to Verilog, Language elements, Lexical Conventions, Value Set, Data types, Modules and ports, Operands, Operators, Expressions, Delays, Compiler Directives, Tasks and Functions, Synthesis and Simulation, Test Benches, Gate-level Modeling, Dataflow Modeling, Behavioral Modelling, Structural Modeling, Mixed Modeling Techniques, Realization of combinational and sequential circuits using Verilog.	**10**	--	--
2	**Programmable Logic devices and their architecture:** Types of Simple programmable logic devices – ROMs, PLAs, PALs, GALs; Complex Programmable Logic Devices, FPGA programming technologies - SRAM, Anti-fuse, EPROM, EEPROM, Flash; FPGA design flow, Programmable Logic blocks, Programmable Interconnects and Programmable I/O bocks in FPGAs, Applications of FPGAs, Microsemi (formerly Actel) ACT series, Xilinx LCA series, Intel (formerly Altera) flex series, Intel Max series.	**10**	--	--
3	**Data Path Design:** Arithmetic Implementation Strategies for VLSI, Bit Serial Arithmetic, Bit Parallel Arithmetic, full adder, Mirror adder, Carry bypass adder, Carry select adder, Carry look ahead adder.	**06**	--	--
4	**VLSI Design Automation**: Brief overview of basic VLSI Design automation concepts, netlist and system partitioning, timing analysis in the context of physical design automation, placement algorithm.	**06**	--	--

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COURSE STRUCTURE

Course Code	**ECV522**			
Course Category	**Core Engineering**			
Course Title	**Embedded Signal Processing**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites:

1. Signals and Systems
2. Digital Signal Processing

Course Objectives:

1. Knowledge (i) Understand digital signal processing operations in frequency domain

2. Skills **(i)** Understand concepts of designing digital filters & its implementations.
(ii) Introduce concepts of iteration bound & data flow graph

3. Attitude (i) Be able to grasp knowledge of wavelet files & Haar 2-band filter bank.

Course Outcomes: After studying this course, students will able to

1. Design FIR & ITR filters for any applications.
2. Design adaptive filter.
3. Develop an algorithm or Architecture for application.
4. Design Haar two band filter bank.
5. Use pipelining and parallel processing in design of high speed/ low power application.

Course Contents:

Introduction to DSP and Filter Design:
Introduction to Digital Signal Processing, Fourier Transform, DFT, DTFT, FFT, STFT Digital Filter Design : IIR, FIR Filter Design, Adaptive Filters, Filter structure.

Haar Wavelet two band filter bank design:
Introduction to wavelet, Haar multiresolution analysis, Haar two band filter banks frequency analysis of Haar two band filter banks, condition for alias cancellation & perfect reconstruction, decomposition and reconstruction of given signal using Haar two band filter bank.

Iteration bound, Pipelining and Parallel Processing:
Iteration bound, representation , data flow graph representation , bound & interaction bound algorithms for computing interaction Bound, pipelining & parallel processing of FIR Filters.

Study of DSP Processors and its Architecture:
DSP Processors, architecture of digital signal processor architecture, fixed point & floating point Format DSP processor, study of processors: TMS 320 C5 XX, TMS 320C67 XX and black Fin.

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Learning Resources:

Reference Books:

1. Sanjit K.Mitra , " Digital Signal Processing: A Computer based approach ", McCraw Hill, 1998 , ISBN 070429537.
2. K.K.Parhi, "VLSI Digital Signal Processing Systems-Design and Implementation," John Wiley & Sons, INC.
3 Raghuveer M.Rao and Ajit S. Bapardikar , Wavelet transforms-Introduction to theory and applications , Pearson Education 2000.
3. K.P. Soman and K.L.Ramchandran, Insight into WAVELETS from theory to practice, Eastern Economy Edition, 2008.
4. Sen M.Kuo and Woon-Seng Gan, "Digital Signal Processors, architectures, implementations, and applications,"Prentice –Hall, ISBN 0130352144.
5. Lawrence R.Rabiner and Bernand Gold, "Theory and application of Digital signal Processing, "Prentice-Hall of India, 2006.
7. I.S.Mallat. "A Wavelet Tour Signal Processing. " Academic press, Second Edition, 1999...L.Cohen," Time -Frequency analysis", Prentce Hall, 1995.
8. G.Strang and T.Q.Nguyen, Wavelets and Filter Banks, "Wellesley-Cambridge Press, Revised edition, 1998.

Web Resources:

Weblinks:

1. http://users.rowan.edu/~polikar/WAVELETS/WTpart1.html (see also Part 2, Part3 and Part 4)
2. *https://www.youtube.com/watch?v=6dFnpz_AEyA*

MOOCs:

1. Course on Fundamentals of wavelets, filter bank and time frequency analysis by Dr. Vikram Gadre, Professor IIT Bombay
   https://onlinecourses.nptel.ac.in/noc17_ee09/preview
2. http://nptel.ac.in/courses/103106114/48
3. Course on DSP by Dr. S. C. Dutta Roy, Professor IIT Delhi
   http://nptel.ac.in/courses/117102060/

Pedagogy:

1. PPT
2. Videos
3. Group Discussion
4. Group Assignments
5. NPTEL Videos

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Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

Term End Examination : 50 Marks (100%)

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	*Lab*	*Assess*
1	**Introduction to DSP and Filter Design:** Introduction to Digital Signal Processing, Fourier Transform, DFT, DTFT, FFT, STFT Digital Filter Design : IIR, FIR Filter Design, Adaptive Filters, Filter structure.	**8**	--	--
2	**Haar Wavelet two band filter bank design:** Introduction to wavelet, Haar multiresolution analysis, Haar two band filter banks frequency analysis of Haar two band filter banks, condition for alias cancellation & perfect reconstruction, decomposition and reconstruction of given signal using haar two band filter bank.	**8**	--	--
3	**Iteration bound, Pipelining and Parallel Processing:** Iteration bound, representation , data flow graph representation , bound & interaction bound algorithms for computing interaction Bound, pipelining & parallel processing of FIR Filters.	**8**	--	--
4	**Study of DSP Processors and its Architecture:** DSP Processors, architecture of digital signal processor architecture, fixed point & floating point Format DSP processor, study of processors: TMS 320 C5 XX, TMS 320C67 XX and black Fin.	**8**	--	--

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COURSE STRUCTURE

Course Code	**ECV523A**			
Course Category	**Elective**			
Course Title	**ANN and Fuzzy Systems (Elective-I)**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites: Calculus, Probability and Statistics

Course Objectives:

Knowledge: **(i)** To get introduced to the basic concepts of soft computing methodology
(ii) To get hands-on experience for problem solving

Skills: **(i)** To develop ANN system design.
(ii) To develop Fuzzy system design.

Attitude: **(i)To** formulate basic Genetic operators
(ii) To understand a dynamical systems approach to machine intelligence.

Course Outcomes:

After completion of this course students will be able to

1. Explain the concepts of neural networks, fuzzy logic & Genetic Algorithms
2. Evaluate problems that are appropriately solved by neural networks & fuzzy logic
3. Design fuzzy system.
4. Design applications in various fields using ANN.

Course Contents:

Artificial Neural Network (ANN)

Overview of Neural Network, ANN Topology, Types of learning, Multilayer Perceptron, RBF, Supervised, Unsupervised Learning algorithm, Neural Network for signal Processing Applications – Audio and ECG.

Fuzzy System

Fuzzy Set Theory - Basic Fuzzy Rules and Fuzzy Reasoning, Fuzzy interference Systems, defuzzification techniques, Adaptive fuzzy systems – Entropy and Subset hood, Applications of Fuzzy in Signal Processing –cruise controller and Air conditioner controller.

Fuzzy-Neural System

Fuzzy neural network, Adaptive Neuro-fuzzy inference systems (ANFIS), Neuro-fuzzy control, Neural-fuzzy applications in pattern recognition, Non-Linear System Identification, Adaptive Noise Cancellation

Genetic Algorithm

Introduction to Genetic Algorithms, Encoding, Fitness function, Reproduction operators, Genetic Modeling, Genetic operators, Cross over, Mutation operator, Ant colony search and Particle Swarm Optimization.

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Learning Resources:

Reference Books:

1. S.R.Jang, C.T.Sun and E.Mizutani, "Neuro-Fuzzy and Soft Computing", PHI 2012,
2. S.Rajasekaran & G.A.Vijayalakshmi PAi, "Neural Networks, Fuzzy Logic and Genetic Algorithms", PHI 2003.
3. Kosko Bart, "Neural Networks and Fuzzy Systems: A Dynamical Systems Approach To Machine Intelligence", PHI, 2000

Supplementary Reading: Notes in the pdf format will be provided

Weblinks: https://www.coursera.org/learn/machine-learning
https://www.datasciencecentral.com/.../top-9-machine-learning-applications-in-real-world

MOOCs: Coursera and NPTEL Lectures

Pedagogy:

Mainly on Power Point Presentation
Problems based 2 tutorials for ANN and GA

Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

Term End Examination : *50 Marks (100%)*

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	Lab	Assess
1	**Artificial Neural Network (ANN)** Overview of Neural Network, ANN Topology, Types of learning, Multilayer Perceptron, RBF, Supervised, Unsupervised Learning algorithm, Neural Network for signal Processing Applications – Audio and ECG.	**8**	--	--
2	**Fuzzy System** Fuzzy Set Theory - Basic Fuzzy Rules and Fuzzy Reasoning, Fuzzy interference Systems, defuzzification techniques, Adaptive fuzzy systems – Entropy and Subset hood, Applications of Fuzzy in Signal Processing –cruise controller and Air conditioner controller.	**8**	--	--
3	**Fuzzy neural network**, Adaptive Neuro-fuzzy inference systems (ANFIS), Neuro-fuzzy control, Neural-fuzzy applications in pattern recognition, Non-Linear System Identification, Adaptive Noise Cancellation	**8**	--	--
4	**Introduction to Genetic Algorithms,** Encoding, Fitness function, Reproduction operators, Genetic Modeling, Genetic operators, Cross over, Mutation operator, Ant colony search and Particle Swarm Optimization.	**8**	--	--

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COURSE STRUCTURE

Course Code	**ECV523B**			
Course Category	**Elective**			
Course Title	**Speech Processing (Elective-I)**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites: Signals & Systems, Digital Signal Processing, Probability and random Process

Course Objectives:

1. To achieve an understanding of speech production and perception.
2. To understand the techniques of speech signal analysis.
3. To achieve an understanding of speech coding and speech enhancement techniques.
4. To understand functioning of automatic speech and speaker recognition systems.

Course Outcomes:

After completion of this course students will be able to

1. Apply the knowledge of speech production system to estimate pitch and formants of speech signals.
2. Analyze speech signals in cepstral domain and represent it in MFCC form.
3. Represent a speech signal for transmission and storage.
4. Analyze designs of systems like Text-To-Speech conversion, Speaker recognition.

Course Contents:

Speech Production and Modeling

Fundamentals of speech science, Speech Production and Perception, Acoustic Phonetics, Classification of sound, Physiological model, Mathematical model

Speech Signal Analysis

Short-Term processing of speech, speech signal parameters, pitch and formants estimation, homomorphic speech signal deconvolution, Cepstral analysis and applications, Linear prediction analysis and applications

Speech Coding and Enhancement

Waveform coding, Speech synthesis, Vocoders, Short-term spectral amplitude techniques for enhancement, Adaptive noise cancelling, Speech quality assessment

Speech Processing Applications

Speech and speaker recognition, Dynamic Time Warping (DTW), Hidden Markov Model (HMM), Text to Speech (TTS) system, Musical Instrument Classification, Aids for the speech and hearing impairments

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Learning Resources:

Reference Books:

1. J. R. Deller, Jr. , J. G. Proakis, J. H. L. Hansen, "Discrete-Time Processing of Speech Signals", IEEE Press, Wiley India, 2011 Reprint.
2. L. R. Rabiner and R.W. Schafer, "Digital Processing of Speech Signals", Prentice Hall, 1978.
3. Thomas F. Quatieri, "Discrete-Time Speech Signal Processing: Principles and Practice", Pearson Education, 2012.
4. Gold and N. Morgan, "Speech and Audio Signal Processing: Processing and perception of speech and music", Wiley, 2000.

Pedagogy:

1. PPT
2. Videos
3. Group Discussion
4. Group Assignments
5. NPTEL Videos

Assessment Scheme:

Class Continuous Assessment (CCA):

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

Term End Examination: *50 Marks (100%)*

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	Lab	Assess
1	**Speech Production and Modeling** Fundamentals of speech science, Speech Production and Perception, Acoustic Phonetics, Classification of sound, Physiological model, Mathematical model	**8**	--	--
2	**Speech Signal Analysis** Short-Term processing of speech, speech signal parameters, pitch and formants estimation, homomorphic speech signal deconvolution, Cepstral analysis and applications, Linear prediction analysis and applications	**8**	--	--
3	**Speech Coding and Enhancement** Waveform coding, Speech synthesis, Vocoders, Short-term spectral amplitude techniques for enhancement, Adaptive noise cancelling, Speech quality assessment	**8**	--	--
4	**Speech Processing Applications** Speech and speaker recognition, Dynamic Time Warping (DTW), Hidden Markov Model (HMM), Text to Speech (TTS) system, Musical Instrument Classification, Aids for the speech and hearing impairments	**8**	--	--

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COURSE STRUCTURE

Course Code	**ECV524**			
Course Category	**Core Engineering**			
Course Title	**Lab Practice-II**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**0**	**0**	**6**	**0+0+3**

Pre-requisites: C/C++, MATLAB, Xilinx, DSP Processor & Code Composer Studio

Course Objectives:

1. To write Verilog codes for modelling various digital logic blocks.
2. To build the complex logic circuit using minimal logic blocks.
3. To understand concepts of designing digital filters & its implementations.
4. To develop ANN & Fuzzy system design.

Course Outcomes:

After completion of this course students will be able to

1. Model digital circuits by using Verilog HDL language.
2. Design and optimize digital logic circuits.
3. Design FIR & ITR filters for any applications.
4. Design applications in various fields using ANN.

Course Contents:

Advanced VLSI Design

Importance of HDLs, Introduction to Verilog, Language elements, Lexical Conventions, Value Set, Data types, Modules and ports, Operands, Operators, Expressions, Delays, Compiler Directives, Tasks and Functions, Synthesis and Simulation, Test Benches, Gate-level Modeling, Dataflow Modeling, Behavioral Modelling, Structural Modeling, Mixed Modeling Techniques, Realization of combinational and sequential circuits using Verilog.

Embedded Signal Processing Introduction to Digital Signal Processing, Fourier Transform, DFT, DTFT, FFT, STFT Digital Filter Design : IIR, FIR Filter Design, Adaptive Filters, Filter structure.

ANN and Fuzzy System Overview of Neural Network, ANN Topology, Types of learning, Multilayer Perceptron, RBF, Supervised, Unsupervised Learning algorithm, Neural Network for signal Processing Applications – Audio and ECG

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Syllabus:

Expt. No.	Title of Experiment	Workload in Hrs		
		Theory	*Lab*	*Assess*
Advanced VLSI Design				
1	Write Verilog HDL code for following examples, simulate, synthesize and implement 1. 4-bit ripple carry counter 2. Traffic signal controller 3. Lift control 4. ADC/DAC interfacing	**--**	**10**	**--**
2	Draw layout for following example and simulate using CAD tool 1. Transmission gate (TG)Full Adder Design: 2. D Flip flop 3. Multiplexer 4. Counter	**--**	**10**	**--**
Embedded Signal Processing				
1	Implementation of circular convolution using FFT and IFFT.	**--**	**4**	**--**
2	Design of Low pass and High Pass FIR filter design using window method.	**--**	**4**	**--**
3	Design of Low pass and High Pass IIR filter using Butterworth & Chebyshev filter for same Specification.	**--**	**4**	**--**
4	Decomposition and reconstruction of a discrete sequence using Haar wavelet.	**--**	**4**	**--**
5	Implementation of filter design using DSP Processor.	**--**	**4**	**--**
ANN & Fuzzy System (Elective-I)				
1	Implement AND, OR, NAND & NOR Gates perceptron network. (with and without MATLAB)	**--**	**4**	**--**
2	Implement XOR gate using BPN and RBF Network.	**--**	**4**	**--**
3	Implement Mamdani Fuzzy Model and Sugeno Fuzzy Model.	**--**	**4**	**--**
4	Implement Fuzzy Inference System (FIS) for realizing basic image processing applications.	**--**	**4**	**--**
5	Design an application of Genetic algorithm using MATLAB toolbox.	**--**	**4**	**--**

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COURSE STRUCTURE

Course Code	**ECV 531**			
Course Category	*Core Engineering*			
Course Title	**System on Chip**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**-**	**--**	**2+0+0**

Pre-requisites:

ECV512 Analog and Digital VLSI Design
ECV521 Advanced VLSI Design

Course Objectives:

At the end of this course, Learners will be able to,

7. **Describe** the architecture of System on Chip (SOC). **(Knowledge)**
8. **Develop** project based on SOC using System C or any HDL language **(Knowledge)**
9. **Select** memory for specific SOC operating system. **(Skill)**
10. **Build** the complex logic circuit using minimal logic blocks. **(Skill)**
11. **Explain** the SOC interconnect architectures. **(Attitude)**
12. **Compare** SOC architectures suitable for current needs. **(Attitude)**

Course Outcomes:

At the end of this course, Learners will be able to,

6. **Outline** the architecture of System and Processor developed by semiconductor vendors. **(CL II)**
7. **Identify** components of SoC. **(CL III)**
8. **Compare** SoC architectures. **(CL IV)**
9. **Choose** SoC architecture for specific application. **(CL VI)**
10. **Explain** SOC Applications and Case Studies developed on SoC platform. **(CL II)**

Course Contents:

Introduction to the SoC Architecture, Processor Architecture: Introduction to Software and Hardware Co-design, System Architecture, Components of the system, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity. Processor Selection for SOC, Basic Concepts in Processor Architecture, Basic Concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers, Branches, More Robust Processors, Vector Processors, VLIW Processors, Superscalar Processors, Processor as IP.

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Memory Design for SOC:
SOC External Memory, Internal Memory, Size of Memory, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for Line Replacement at Miss Time, Other types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to Real Translation, SOC Memory System, Models of Simple Processor – Memory Interaction.

Interconnect, Customization and Configuration:
Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration.

SoCs, Application Studies / Case Studies: SOC Design approach, AES: Algorithms and Requirements, AES: Design and evaluation, Image compression: JPEG Compression, Image compression: JPEG System for Digital Still Camera, Video Compression: MPEG and H.26X Requirements, Video Compression: H.264 Acceleration Designs.

Learning Resources:

Reference Books:

1. Michael J. Flynn and Wayne Luk, "Computer System Design: System-On-Chip", Wiely India, 2011.
2. Wayne Wolf, "Modern VLSI Design – System – on – Chip Design", Prentice Hall, 3rd Edition, 2008.
3. Ricardo Reis, "Design of System on a Chip: Devices and Components", Springer. 1st Ed., 2004.
4. Prakash Rashinkar, Peter Paterson and Leena Singh L, "System on Chip Verification – Methodologies and Techniques", Kluwer Academic Publishers 2001.
5. Youn-Long Steve Lin, "Essential Issues in SOC Design, Designing Complex Systems-on-Chip", Springer, 2006.

Supplementary Reading:

Web Resources:

Web links:

3. https://www.xilinx.com/products/silicon-devices/soc/zynq-7000.html
4. https://www.altera.com/products/soc/overview/soc-resource-guide/Introduction.html
5. https://developer.arm.com/products/processors/cortex-a/cortex-a9

MOOCs:

6. https://www.mooc-list.com/course/soc-verification-using-system-verilog-udemy

Pedagogy:

- Power Point Presentation
- Demonstration

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- Video
- Interactive

Assessment Scheme:

Class Continuous Assessment (CCA) – 50 Marks

Assignments	Test	Presentations	Case study	MCQ	Oral	Any other
40%	40%	0%	0%	0%	0%	20%

Laboratory Continuous Assessment (LCA)

Practical	Oral based on practical	Site Visit	Mini Project	Problem based Learning	Any other
0%	0%	0%	0%	0%	0%

Term End Examination: 50 Marks

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	*Lab*	*Assess*
1	**Introduction to the SOC Architecture, Processor Architecture:** Introduction to Software and Hardware Co-design, System Architecture, Components of the system, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity. Processor Selection for SOC, Basic Concepts in Processor Architecture, Basic Concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers, Branches, More Robust Processors, Vector Processors, VLIW Processors, Superscalar Processors, Processor as IP.	**10**	**0**	**0**
2	**Memory Design for SOC:** SOC External Memory, Internal Memory, Size of Memory, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for Line Replacement at Miss Time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to Real Translation, SOC Memory System, Models of Simple Processor – Memory Interaction.	**08**	**0**	**0**
3	**Interconnect, Customization and Configuration:** Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration.	**08**	**0**	**0**
4	**Application Studies / Case Studies:** SOC Design approach, AES: Algorithms and Requirements, AES: Design and evaluation, Image compression: JPEG Compression, Image compression: JPEG System for Digital Still Camera, Video Compression: MPEG and H.26X Requirements, Video Compression: H.264 Acceleration Designs.	**06**	**0**	**0**

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COURSE STRUCTURE

Course Code	**ECV532A**			
Course Category	**Elective**			
Course Title	**Mixed Signal CMOS Design (Elective-II)**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites: Analog and Digital CMOS Design, Advanced VLSI Design

Course Objectives:

1. To provide the background of mixed signal issues in CMOS technologies
2. To understand the operation of basic analog CMOS cells.
3. To study different types of data converter circuits
4. To introduce fundamentals of RF circuit design

Course Outcomes:

After completion of this course students will be able to

1. Explain mixed signal issues, analog testing and layout issues in CMOS technologies
2. Analyze analog and digital CMOS cells
3. Demonstrate the knowledge of data converters
4. Understand concepts of RF circuits

Course Contents:

Introduction to Mixed Signal CMOS

Introduction to analog VLSI and mixed signal issues in CMOS technologies, Analog Interconnects, Analog Testing and Layout issues

Mixed Signal Circuit

Frequency Synthesizers and Phased lock-loop. Non-linear analog blocks: Comparators, Charge-pump circuits and Multipliers.

Data Converters

Data converters, Successive approximation ADCs, Dual slope ADCs, High-speed ADCs (e.g. flash ADC, pipeline ADC and related architectures), High-resolution ADCs (e.g. delta-sigma converters) Mixed- Signal layout, Interconnects.

Filters

Review of continuous-time filters, Discrete-time filters, Analog and discrete-time signal processing, analog integrated continuous-time and discrete-time (switched-capacitor) filters, Introduction to RF Electronics, Basic concepts in RF design

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Learning Resources:

Reference Books:

1. R. Jacob Baker, "CMOS mixed-signal circuit design", Wiley India, IEEE press, reprint 2008.
2. Rudy V. DePlassche, " CMOS Integrated ADCs and DACs", Springer, Indian edition, 2005
3. Behzad Razavi, "Design of analog CMOS integrated circuits", McGraw-Hill, 2003.
4. R. Jacob Baker, "CMOS circuit design, layout and simulation", Revised second edition, IEEE press, 2008.
5. B. Razavi, "RF Microelectronics", Prentice-Hall PTR, 1998.

Pedagogy:

1. Power Point Presentation
2. Videos
3. Group Discussion

Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

End Semester Exam: 50 Marks (100%)

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	*Lab*	*Assess*
1	**Introduction to Mixed Signal CMOS** Introduction to analog VLSI and mixed signal issues in CMOS technologies, Analog Interconnects, Analog Testing and Layout issues	**8**	--	--
2	**Mixed Signal Circuit** Frequency Synthesizers and Phased lock-loop. Non-linear analog blocks: Comparators, Charge- pump circuits and Multipliers.	**8**	--	--
3	**Data Converters** Data converters, Successive approximation ADCs, Dual slope ADCs, High-speed ADCs (e.g. flash ADC, pipeline ADC and related architectures), High-resolution ADCs (e.g. delta-sigma converters) Mixed- Signal layout, Interconnects.	**8**	--	--
4	**Filters** Review of continuous-time filters, Discrete-time filters, Analog and discrete-time signal processing, analog integrated continuous-time and discrete-time (switched-capacitor) filters, Introduction to RF Electronics, Basic concepts in RF design	**8**	--	--

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COURSE STRUCTURE

Course Code	**ECV532B**			
Course Category	**Elective**			
Course Title	**Wireless Sensor Networks (Elective-II)**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites: Wireless Communication, Embedded system

Course Objectives:

1. To study the architecture of WSN network.
2. To study the physical layer related aspects of WSN.
3. To study the power management issues in wireless communication.
4. To understand security aspects in WSN system.
5. To study various operating systems in WSN.

Course Outcomes:

After completion of this course students will be able to

1. The student will understand the architecture of WSN network.
2. The student will understand the physical layer related aspects of WSN network.
3. The student will exhibit the knowledge of power management in wireless communication systems.
4. The student will exhibit the knowledge of security aspects of WSN systems.

Course Contents:

Overview of Wireless Sensor Networks

Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks

Architectures

Single-Node Architecture - Hardware Components, Energy Consumption of Sensor nodes, Operating Systems and Execution Environments, Network Architecture - Sensor Network Scenarios, Optimization Goals and Figures of Merit, Gateway Concepts.

Networking Sensors

Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Address and Name Management, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing.

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Infrastructure Establishment, Platforms and Tools

Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control, Sensor Node Hardware – Berkeley Motes, Programming Challenges, Node-level software platforms, Node-level Simulators, State-centric programming.

Learning Resources:

Reference Books:

1. Holger Karl & Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks", John Wiley, 2005.
2. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
3. Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks Technology, Protocols, and Applications", John Wiley, 2007.
4. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003

Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

End Semester Exam: This will cover entire syllabus: *50 Marks (100%)*

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	*Lab*	*Assess*
1	**Overview of Wireless Sensor Networks** Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks	**8**	--	--
2	**Architectures** Single-Node Architecture - Hardware Components, Energy Consumption of Sensor nodes, Operating Systems and Execution Environments, Network Architecture - Sensor Network Scenarios, Optimization Goals and Figures of Merit, Gateway Concepts.	**8**	--	--
3	**Networking Sensors** Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Address and Name Management, Assignment of MAC Addresses, Routing Protocols-Energy-Efficient Routing, Geographic Routing.	**8**	--	--
4	**Infrastructure Establishment, Platforms and Tools** Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control, Sensor Node Hardware – Berkeley Motes, Programming Challenges, Node-level software platforms, Node-level Simulators, State-centric programming.	**8**	--	--

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COURSE STRUCTURE

Course Code	**ECV533A**			
Course Category	**Elective**			
Course Title	**Image Processing and Computer Vision(Ele.-III)**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites: Appiled Physics, Digital Signal Processing, Multirate DSP

Course Objectives:

1. Understand visual processing from both "bottom-up" (data oriented) and "top-down" (goals oriented) perspectives
2. Decompose visual tasks into sequences of image analysis operations, presentations, specific algorithms, and inference principles
3. Build computer systems that analyze and process images automatically for computer vision applications
4. Develop the practical skills necessary to build computer vision applications

Course Outcomes:

After completion of this course students will be able to

1. Understand camera optics and specifications
2. Solve mid -level image processing problems using techniques like filtering and feature detection
3. Analyze high level computer vision problems using image segmentation, registration, recognition, clustering
4. Design and Build algorithms that analyze and process images automatically for computer vision applications

Course Contents:

An Introduction to the Concepts in Image Processing

Cameras and projection models, Low-level vision topics filtering and feature detection, Mid-level vision topics: Feature descriptor, Segmentation and clustering, Image compression

Image Registration and Recognition

Geometric transform, Image registration, Types of image registration, Optimization techniques in image registration, Soft computing in image processing

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Stereo Correspondence and Applications

Epipolar geometry, Techniques of stereo correspondence, Multi-view stereo, Depth estimation, Applications of computer vision

3D Reconstruction

Shape from texture, Shading, focus, Active range finding, Surface representations, Point based representations, Volumetric representations, Model based reconstruction, Image based rendering.

Learning Resources:

Reference Books:

1. Richard Szeliski, "Computer Vision Algorithms and Applications", Springer, 2011.
2. Luigi Landini, Vincenzo Positano, Maria Santarelli, "Advanced Image Processing in Magnetic Resonance Imaging" , CRC Press, 2005
3. U Qidwai, C Chen, "Digital Image Processing an Algorithmic Approach with MATLAB", CRC Press, 2009
4. Al Bovik, "Handbook of Digital Image and Video Processing", Academic Press , June 2005

Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

End Semester Exam: 50 Marks (100%)

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	*Lab*	*Assess*
1	**An Introduction to the Concepts in Image Processing** Cameras and projection models, Low-level vision topics filtering and feature detection, Mid-level vision topics: Feature descriptor, Segmentation and clustering, Image compression	**8**	--	--
2	**Image Registration and Recognition** Geometric transform, Image registration, Types of image registration, Optimization techniques in image registration, Soft computing in image processing	**8**	--	--
3	**Stereo Correspondence and Applications** Epipolar geometry, Techniques of stereo correspondence, Multi-view stereo, Depth estimation, Applications of computer vision	**8**	--	--
4	**3D Reconstruction** Shape from texture, Shading, focus, Active range finding, Surface representations, Point based representations, Volumetric representations, Model based reconstruction, Image based rendering.	**8**	--	--

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COURSE STRUCTURE

Course Code	**ECV533B**			
Course Category	**Elective**			
Course Title	**CUDA Architecture and Programming (Ele.-III)**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites: Computer organization & architecture

Course Objectives:

1. To create awareness about parallel computing and GPU
2. To learn CUDA architecture and Programming model
3. To explore different memory models of CUDA
4. To understand various case studies and CUDA tools.

Course Outcomes:

After completion of this course students will be able to

1. Understand parallel computing and GPU
2. Develop programs in CUDA C.
3. Demonstrate different memory models of CUDA.
4. Understand various CUDA tools.

Course Contents:

Introduction to GPU and Parallel Computing

History of GPUs leading to their use and design for HPC. Introduction to GPU computing, motivation, Introduction to CUDA, Applications of CUDA, Development Environment, CUDA C, Kernel call, Passing Parameters, Querying Devices, Using Device Properties.

Compute Unified Device Architecture (CUDA)

CUDA Architecture, CUDA programming model, execution model, Thread organization: Concept of grid, Block and thread, Thread index generation, warp; CUDA example programs (Vector dot product, Vector-Matrix multiplication and etc).

CUDA Memory Models

Introduction to global, shared, Local memories, Usage of cache, Texture cache, Constant memory, Memory banks and bank conflicts, Memory coalescing, CUDA structure and API details, CUDA example programs for memory models.

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Case Study and Tools

Introduction Modern GPU architecture case study like NVIDIA Fermi Tesla C2050/Kepler /Pascal, Introduction to CUDA Tools: Recheck and & Visual Profiler.

Learning Resources:

Reference Books:

1. David Kirk, Wen-mei Hwu © ELSEVIER Inc., "CUDA: Programming Massively Parallel Processors: A Hands-On Approach"
2. Jason Sanders and Edward Kandrot –Addison Wesley, "CUDA by Example: An Introduction to General-Purpose GPU Programming"
3. Kai Hwong, "Advanced computer architecture", Tata McGraw-Hill Edition, 2001.
4. Shane Cook, "CUDA Programming: A Developer's Guide to parallel computing with GPUs"

Pedagogy:

1. Power Point Presentation
2. Videos
3. Group Discussion

Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

End Semester Exam: 50 Marks (100%)

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	*Lab*	*Assess*
1	**Introduction to GPU and Parallel Computing** History of GPUs leading to their use and design for HPC. Introduction to GPU computing, motivation, Introduction to CUDA, Applications of CUDA, Development Environment, CUDA C, Kernel call, Passing Parameters, Querying Devices, Using Device Properties.	**8**	--	--
2	**Compute Unified Device Architecture (CUDA)** CUDA Architecture, CUDA programming model, execution model, Thread organization: Concept of grid, Block and thread, Thread index generation, warp; CUDA example programs (Vector dot product, Vector-Matrix multiplication and etc).	**8**	--	--
3	**CUDA Memory Models** Introduction to global, shared, Local memories, Usage of cache, Texture cache, Constant memory, Memory banks and bank conflicts, Memory coalescing, CUDA structure and API details, CUDA example programs for memory models.	**8**	--	--
4	**Case Study and Tools** Introduction Modern GPU architecture case study like NVIDIA Fermi Tesla C2050/Kepler /Pascal, Introduction to CUDA Tools: Recheck and & Visual Profiler.	**8**	--	--

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Course Code	**ECV534**			
Course Category	**Core Engineering**			
Course Title	**Lab Practice-III**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**0**	**0**	**6**	**0+0+3**

Pre-requisites: MATLAB, Xilinx, OpenCV, Microwind

Lab assignments of SOC (any five)

1. HDL based design of a simple processor- implementation, testing and verification
2. Estimating power consumption of a simple design
3. Implement CMOS layout which will generate glitch also design a RTL by Writing VHDL which will generate glitch and also measure it using electronic test equipment.
4. NISC toolkit – installation and experimentation -HDL code synthesis and C based approach for design
5. Optimization of area, speed, power parameters for high speed operation
6. Implement any data logging system as a co-design by Interfacing FPGA & μC 8051

Lab assignments of Wireless Sensor Networks

1. Sensing data using wireless nodes
2. Design and study ad-hoc wireless network using 3 node scenario
3. Design and study ad-hoc wireless network having mobility of node
4. Design and study ad-hoc wireless multi node network and measure performance parameters
5. Design and study any one application like Zigbee automation wireless network

Lab assignments of Image Processing and Computer Vision

1. Camera Models, Camera Calibration
2. Computer vision application based on segmentation / clustering
3. Computer vision application based on Image registration / Compression
4. Computer vision application based on Disparity estimation / Depth map generation / 3D modeling

Lab assignments of CUDA Architecture and Programming (Any Four)

1. Display device properties by using device Query program.
2. Write a program to perform vector addition using CUDA. Vector size should be greater than 10000 values.
3. Write a program to perform dot product using CUDA programming.
4. Write a program to perform matrix multiplication using shared memory in CUDA.
5. Measure GPU time and speed up for squaring an array using CUDA programming

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Assessment Scheme:

Continuous Assessment Tools

Laboratory Continuous Assessment (LCA)

Performance in Experiment	Result Analysis & Conclusion	Journal/Report	Attendance/ Discipline/Initiative	Total
15 (30 %)	15 (30%)	10 (20%)	10 (20%)	50 (100%)

- **Practical / Oral Exam based on submission at the end of trimester: 50 Marks (100%)**

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Syllabus:

Expt. No.	Title of Experiment	Workload in Hrs		
		Theory	*Lab*	*Assess*
System On Chip				
1	HDL based design of a simple processor- implementation, testing and verification		**4**	
2	Estimating power consumption of a simple design		**4**	
3	Implement CMOS layout which will generate glitch also design a RTL by Writing VHDL which will generate glitch and also measure it using electronic test equipment.		**4**	
4	NISC toolkit – installation and experimentation -HDL code synthesis and C based approach for design		**4**	
5	Optimization of area, speed, power parameters for high speed operation		**4**	
6	Implement any data logging system as a co-design by Interfacing FPGA & µC 8051			
Wireless Sensor Networks				
1	Sensing data using wireless nodes		**4**	
2	Design and study ad-hoc wireless network using 3 node scenario		**4**	
3	Design and study ad-hoc wireless network having mobility of node		**4**	
4	Design and study ad-hoc wireless multi node network and measure performance parameters		**4**	
5	Design and study any one application like Zigbee automation wireless network		**4**	
Image Processing and Computer Vision				
1	Camera Models, Camera Calibration		**4**	
2	Computer vision application based on segmentation / clustering		**4**	
3	Computer vision application based on Image registration / Compression		**4**	
4	Computer vision application based on Disparity estimation / Depth map generation / 3D modeling		**4**	
CUDA Architecture and Programming				
1	Display device properties by using device Query program.		**4**	
2	Write a program to perform vector addition using CUDA. Vector size should be greater than 10000 values.		**4**	
3	Write a program to perform dot product using CUDA programming.		**4**	
4	Write a program to perform matrix multiplication using shared memory in CUDA.		**4**	
5	Measure GPU time and speed up for squaring an array using CUDA programming		**4**	

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COURSE STRUCTURE

Course Code	**ECV535**			
Course Category	**Core Engineering**			
Course Title	**Seminar I**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**0**	**0**	**4**	**0+0+2**

Course Objectives:

1. To refer articles published in current journals in interdisciplinary area for choosing their seminar topics.
2. To review minimum of 5 to 6 research papers relevant to the topic chosen, in addition to standard textbooks, handbooks, etc.
3. To communicate technical information in a professional manner by written and oral means.

Course Outcomes:

After completion of this course students will be able to

1. Select a latest interdisciplinary topic of interest
2. Undertake a critical review of the literature on the chosen topic
3. Prepare and present a technical report

Seminar I should be on a **latest interdisciplinary topic** of student's own choice approved by the concerned Guide. Student should present their seminar topic and submit a seminar report in standard format, certified by concerned authority.

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COURSE STRUCTURE

Course Code	**ECV611**			
Course Category	**Core Engineering**			
Course Title	**Testing and Testability**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites: Analog and Digital VLSI Design, Embedded System

Course Objectives:

1. To create understanding of the fundamental concepts of fault-tolerant digital System
2. To develop skills in modeling and Simulations
3. To know various testing methods for detection of faults
4. To learn self-testing techniques for memory, processor and PLA

Course Outcomes:

After completion of this course students will be able to

1. Understand concepts of fault-tolerant digital systems.
2. Model and simulate fault-tolerant digital systems.
3. Apply various testing methods for detection of faults
4. Use self-testing techniques for memory, processor and PLA

Course Contents:

Modeling and Logic Simulation

Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models.

Fault Modeling and Fault Simulation

Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits. Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms, Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods

Testing for Single Stuck Fault and Design for Testability

Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain based testing method, D-algorithm procedure, Problems, PODEM Algorithm, Problems on PODEM Algorithm, FAN Algorithm, Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan based design

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Testability

Classical scan based design, System level DFT approaches, Test pattern generation for BIST, and Circular BIST, BIST Architectures, and Testable memory design-Test algorithms-Test generation for Embedded RAMs.

Learning Resources:

Reference Books:

1. M. Abramovici, M. Breuer, and A. Friedman, "Digital Systems Testing and Testable Design, IEEE Press, 1990.
2. Stroud, "A Designer's Guide to Built-in Self-Test", Kluwer Academic Publishers, 2002
3. M. Bushnell and V. Agrawal, "Essentials of Electronic Testing for Digital, Memory &Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000
4. Agrawal and S.C. Seth, "Test Generation for VLSI Chips", Computer SocietyPress.1989

Pedagogy:

1. Power Point Presentation
2. Videos
3. Group Discussion
4. Group Proposals

Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

End Semester Exam: 50 Marks (100%)

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	*Lab*	*Assess*
1	**Modeling and Logic Simulation** Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models	**8**	--	--
2	**Fault Modeling and Fault Simulation** Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits. Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms, Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods	**8**	--	--
3	**Testing for Single Stuck Fault and Design for Testability** Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain based testing method, D-algorithm procedure, Problems, PODEM Algorithm, Problems on PODEM Algorithm, FAN Algorithm, Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan based design	**8**	--	--
4	**Testability** Classical scan based design, System level DFT approaches, Test pattern generation for BIST, and Circular BIST, BIST Architectures, and Testable memory design-Test algorithms-Test generation for Embedded RAMs.	**8**	--	--

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COURSE STRUCTURE

Course Code	**ECC612**			
Course Category	**Core Engineering**			
Course Title	**Artificial Intelligence Techniques and Applications**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites: Fundamentals of Linear Algebra and Probability theory.

Course Objectives:

1. To provide insights of Artificial Intelligence and Data mining Techniques.
2. To explore various applications of AI and data mining.

Course Outcomes: After completion of this course students will be able to

1. Design intelligent agent for problem solving.
2. Understand various soft computing techniques.
3. Formulate and solve any real world problem of classification, clustering and prediction.
4. Apply AI techniques in Data mining applications.

Course Contents:

- **Artificial Intelligence:** Problem solving, Knowledge, reasoning, toy and real world problems, Learning from examples.
- **Soft Computing Techniques:** Neural Networks, Multilayer Perceptrons, Self Organizing Maps, Deep Learning Networks. Introduction to Fuzzy Logic and Genetic Algorithm.
- **Classification and Cluster Analysis:** Concepts, advanced methods, outlier detection.
- **Data mining :** Introduction to data mining, getting to know your data, Data Pre-processing, Data warehousing, mining frequent patterns, use of AI in data mining , Applications of Data mining.

Learning Resources:

Reference Books:

1. Stuart J.Russelland PeterNorvig, "Artificial Intelligence A Modern Approach" ,3rd edition, Pearson Education.
2. JiaweiHan ,MichelineKamber and Jian Pei, "Data Mining Concepts and Techniques", Elsevier.

Supplementary Reading:

1. Bing Liu, "Web Data Mining Exploring Hyperlinks Contents , and Usage Data" Springer International Edition.
2. KishanMehrotra ,Chilukuri Mohan and Sanjay Ranka, "Elements of Artificial Neural Networks", MIT Press.

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Pedagogy:

- Power Point Presentations, Videos
- Co-teaching
- Group Activities

Assessment Scheme:

Class Continuous Assessment (CCA) (50 Marks)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

Term End Examination : (50 Marks) (100%)

Syllabus :

Module No.	Contents	Workload in Hrs		
		Theory	*Lab*	*Assess*
1	**Artificial Intelligence:**Problem solving, Knowledge, reasoning, toy and real world problems, Learning from examples.	**8**		
2	**Soft Computing Techniques:**Neural Networks, Multilayer Perceptrons, Self Organizing Maps, Deep Learning Networks. Introduction to Fuzzy Logic and Genetic Algorithm.	**8**		
3	**Classification and Cluster Analysis:** Concepts, advanced methods, outlier detection.	**8**		
4	**Data mining :** Introduction to data mining, getting to know your data, Data Pre-processing, Data warehousing,mining frequent patterns, use of AI in data mining , Applications of Data mining.	**8**		

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COURSE STRUCTURE

Course Code	**ECV613A**			
Course Category	**Elective**			
Course Title	**Economics for Engineering (Elective-IV)**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites: Business Management, Economics

Course Objectives:

1. To teach the concepts of engineering economic analysis and its role in solving problems.
2. To provide engineers with the tools needed for rigorous presentation of the effect of the time value of money on engineering decision making.
3. To acquaint with Inflation, deflation, depreciation and inflation and its effect on Market

Course Outcomes:

After completion of this course students will be able to

1. Define, estimate and analyze engineering project costs
2. Develop, evaluate, and compare engineering project cash flows
3. Formulate and apply interest factors to real life engineering problems
4. Develop and apply mathematical models describing real life cash flows and time value of money
5. Discuss and solve advanced economic engineering analysis problems including taxation and inflation

Course Contents:

Introduction to Engineering Economics

Money as a Means of Commerce, Improving the Economics of Projects, Managing Costs and Profits, Micro and Macroeconomics, Relationship between science, Engineering, Technology and economic development, Production Possibility Curve, Nature of Economic Law.

Time Value of Money

Definition of Interest, Definition of Engineering Economic Terms, Cash Flow Diagrams, Fiscal and Monetary Policy, LPG, GATT, Central Bank- RBI; its functions, Concepts; CRR, Bank rate, Repo rate, Reverse repo rate, SLR

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Engineering Costs & Estimation

Fixed, Variable, Marginal & Average Costs, Sunk Costs, Opportunity Costs, Recurring And Nonrecurring Costs, Incremental Costs, Cash Costs vs Book Costs, Life-Cycle Costs; Types Of Estimate, Estimating Models - Per- Unit Model, Segmenting Model, Cost Indexes, Power-Sizing Model, Improvement & Learning Curve, Benefits.

Depreciation

Basic Aspects, Deterioration & Obsolescence, Depreciation and Expenses, Types of Property, Depreciation Calculation Fundamentals, Depreciation and Capital Allowance Methods, Straight-Line, Depreciation Declining Balance Depreciation, Inflation and Price change

Learning Resources:

Reference Books:

1. James L.Riggs, David D. Bedworth, Sabah U. Randhawa, " Engineering Economics 4e", McGraw-Hill
2. Chan S. Park, "Contemporary Engineering Economics, 5th ed.", Pearson Prentice Hall
3. Donald Newnan, Ted Eschembach, Jerome Lavelle, "Engineering Economics Analysis", OUP
4. John A. White, Kenneth E.Case,David B.Pratt, "Principle of Engineering Economic Analysis" John Wiley
5. Pravin Kumar, "Fundamentals of Engineering Economics", John Wiley.

Pedagogy:

1. Power Point Presentation
2. Videos
3. Group Discussion
4. Group Proposals

Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

End Semester Exam: 50 Marks (100%)

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	*Lab*	*Assess*
1	**Introduction to Engineering Economics** Money as a Means of Commerce, Improving the Economics of Projects, Managing Costs and Profits, Micro and Macroeconomics, Relationship between science, Engineering, Technology and economic development, Production Possibility Curve, Nature of Economic Law.	**8**	--	--
2	**Time Value of Money** Definition of Interest, Definition of Engineering Economic Terms, Cash Flow Diagrams, Fiscal and Monetary Policy, LPG, GATT, Central Bank- RBI; its functions, Concepts; CRR, Bank rate, Repo rate, Reverse repo rate, SLR	**8**	--	--
3	**Engineering Costs & Estimation** Fixed, Variable, Marginal & Average Costs, Sunk Costs, Opportunity Costs, Recurring And Nonrecurring Costs, Incremental Costs, Cash Costs vs Book Costs, Life-Cycle Costs; Types Of Estimate, Estimating Models - Per- Unit Model, Segmenting Model, Cost Indexes, Power-Sizing Model, Improvement & Learning Curve, Benefits.	**8**	--	--
4	**Depreciation** Basic Aspects, Deterioration & Obsolescence, Depreciation and Expenses, Types of Property, Depreciation Calculation Fundamentals, Depreciation and Capital Allowance Methods, Straight-Line, Depreciation Declining Balance Depreciation, Inflation and Price change	**8**	--	--

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COURSE STRUCTURE

Course Code	**ECV613B**			
Course Category	**Elective**			
Course Title	**Automotive Embedded Systems (Elective-IV)**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**3**	**0**	**0**	**2+0+0**

Pre-requisites: Basic Mechanical Engg., Microcontrollers, Control System

Course Objectives:

1. To acquaint with the concepts of Automotive Electronics in embedded systems.
2. To study sensors and actuators used in automotive electronics.
3. To review role of Microcontrollers in ECU design.
4. To design and model various automotive control systems.
5. To understand various communication systems used in automotive electronics.

Course Outcomes:

After completion of this course students will be able to

1. Obtain an overview of automotive components, subsystems, design cycles, communication protocols
2. Interface automotive sensors and actuators with microcontrollers
3. Develop, simulate and integrate control algorithms for ECUs with hardware

Course Contents:

Vehicle Functional Domains and Automotive industry overview

Overview of Automotive industry, Introduction to modern automotive systems and need for electronics in automobiles, Spark and Compression Ignition Engines, Automotive transmissions, Safety Systems in Automobiles.

Automotive Sensors and Actuators

Airflow Rate Sensor, Pressure Measurement Sensor, Engine Crank Position sensor, Throttle angle sensor, Temperature Sensor. Sensors for Engine feedback control. Engine control actuators, Electric actuators.

Embedded system for automotive domain, Communication protocols

Microcontrollers/Microprocessors in Automotive domain, Critical review of microprocessor, Understanding various architectural attributes relevant to automotive applications, Automotive grade processors: Renessa, Quorivva, Infineon, Understanding and working on tool chains for different processors, Engine Maps and tables, Communication protocols: CAN, LIN, Flex Ray, MOST.

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Automotive Control Systems and Model Based Development:
Control system approach in Automotive, Model-Based Design for a small system - Motor Model, Generator Model, Controller Model, Real time simulations on target boards

Learning Resources:

Reference Books:

1. Williams. B. Ribbens: "Understanding Automotive Electronics", 6th Edition, Elsevier Science, Newnes Publication, 2003.
2. Robert Bosch: " Automotive Electronics Handbook", John Wiley and Sons, 2004.
3. Marc E. Herniter and Zac Chambers, "Introduction to Model Based System Design", Rose-Hulman Institute of Technology
4. Ronald K Jurgen, "Automotive Electronics Handbook", 2nd Edition, McGraw- Hill, 1999
5. James D. Halderman, "Automotive Electricity and Electronics", PHI Publication

Pedagogy:

1. Power Point Presentation
2. Videos
3. Group Discussion
4. Demonstration

Assessment Scheme:

Class Continuous Assessment (CCA)

Assignments	Mid Term Test	Attendance/ Discipline/ Initiative/ Behavior	Total
20 (40%)	20 (40%)	10 (20%)	50 (100%)

End Semester Exam: 50 Marks (100%)

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Syllabus:

Module No.	Contents	Workload in Hrs		
		Theory	*Lab*	*Assess*
1	**Vehicle Functional Domains and Automotive industry overview** Overview of Automotive industry, Introduction to modern automotive systems and need for electronics in automobiles, Spark and Compression Ignition Engines, Automotive transmissions, Safety Systems in Automobiles.	**8**	**--**	**--**
2	**Automotive Sensors and Actuators** Airflow Rate Sensor, Pressure Measurement Sensor, Engine Crank Position sensor, Throttle angle sensor, Temperature Sensor. Sensors for Engine feedback control. Engine control actuators, Electric actuators.	**8**	**--**	**--**
3	**Embedded system for automotive domain, Communication protocols** Microcontrollers/Microprocessors in Automotive domain, Critical review of microprocessor, Understanding various architectural attributes relevant to automotive applications, Automotive grade processors: Renessa, Quorivva, Infineon, Understanding and working on tool chains for different processors, Engine Maps and tables, Communication protocols: CAN, LIN, Flex Ray, MOST.	**8**	**--**	**--**
4	**Automotive Control Systems and Model Based Development:** Control system approach in Automotive, Model-Based Design for a small system - Motor Model, Generator Model, Controller Model, Real time simulations on target boards	**8**	**--**	**--**

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COURSE STRUCTURE

Course Code	**ECV614**			
Course Category	**Core Engineering**			
Course Title	**Lab Practice-IV**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**0**	**0**	**6**	**0+0+3**
Pre-requisites: MATLAB,Microwind,Xilinx				

Course Contents:

Lab assignments of Testing and Testability

1. Design event driven simulation model using VLSI simulation tool.
2. Implement Serial/ parallel/Deductive fault simulation algorithms
3. Testing of combinational and sequential circuit.
4. Simulate a single input signature analyzer for given characteristic equation and input sequence
5. Implementation of RAM using FPGA

Lab assignments/experiments for Artificial Intelligence Techniques and Applications

Implement a Mini-project solving real world problems involving tasks like classification, clustering or prediction.

1. Introduction to various AI and Data Mining tools for implementing mini projects.
2. Implementation of toy problems on the tools.
3. Mini-project problem formulation and selection of proper methodology.
4. Data collection, visualization and understanding trends in data by plotting it if required.
5. Implement the required and alternate algorithm for the selected application and test the performance of the same.
6. Compare the performance of the two algorithms implemented using measureable parameters like classification rate, kappa index, confusion matrix, sensitivity and specificity, whichever is applicable for the design.

Lab assignments of Economics for Engineering

Case Studies:

1. Discuss effect of GST in Capital Market, Consumer Market and Inflation
2. Discuss the role of Fiscal and Monetary Policy of Government of India.
3. Engineering and economic analysis for climate change adaption
4. New US govt. Foreign Policy in the development of Global economy

Lab assignments of Automotive Embedded Systems

1. Demonstration of the automotive components and subsystems.
2. Modelling examples using MATLAB Simulink.
3. Integrating the control algorithms on target hardware.
4. OBD-II Demonstration.

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Pedagogy:

1. Power Point Presentation
2. Videos
3. Group Discussion
4. Simulation

Assessment Scheme:

Laboratory Continuous Assessment:

Performance in Experiment	Result Analysis & Conclusion	Journal/Report	Attendance/ Discipline/Initiative	Total
15 (30 %)	15 (30%)	10 (20%)	10 (20%)	50 (100%)

- **Practical / Oral Exam based on submission at the end of trimester 50 marks(100 %)**

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Syllabus:

Expt. No.	Title of Experiment	Workload in Hrs		
		Theory	*Lab*	*Assess*
Testing and Testability				
1	Design event driven simulation model using VLSI simulation tool.		**4**	
2	Implement Serial/ parallel/Deductive fault simulation algorithms		**4**	
3	Testing of combinational and sequential circuit.		**4**	
4	Simulate a single input signature analyzer for given characteristic equation and input sequence		**4**	
5	Implementation of RAM using FPGA		**4**	
Artificial Intelligence Techniques and Applications				
1	Introduction to various AI and Data Mining tools for implementing mini projects.		**4**	
2	Implementation of toy problems on the tools.		**4**	
3	Mini-project problem formulation and selection of proper methodology.		**4**	
4	Data collection, visualization and understanding trends in data by plotting it if required.		**4**	
5	Implement the required and alternate algorithm for the selected application and test the performance of the same.		**4**	
6	Compare the performance of the two algorithms implemented using measureable parameters like classification rate, kappa index, confusion matrix, sensitivity and specificity, whichever is applicable for the design		**4**	
Economics for Engineering				
1	Discuss effect of GST in Capital Market, Consumer Market and Inflation		**4**	
2	Discuss the role of Fiscal and Monetary Policy of Government of India.		**4**	
3	Engineering and economic analysis for climate change adaption		**4**	
4	New US govt. Foreign Policy in the development of Global economy		**4**	
Automotive Embedded Systems				
1	Demonstration of the automotive components and subsystems.		**4**	
2	Modelling examples using MATLAB Simulink.		**4**	
3	Integrating the control algorithms on target hardware.		**4**	
4	OBD-II Demonstration		**4**	

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COURSE STRUCTURE

Course Code	**ECV615**			
Course Category	**Core Engineering**			
Course Title	**Project Stage I Seminar**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**0**	**0**	**4**	**0+0+2**

Course Objectives:

1. To make comprehensive use of the technical knowledge gained from previous courses.
2. Identify a problem through literature survey in the selected project domain
3. To apply project management skills such as planning of work, procuring parts, and documenting expenditures and working within the timeline.

Course Outcomes:

After completion of this course students will be able to

1. Identify a suitable project/problem statement making use of the technical knowledge gained from previous courses
2. Collect and disseminate information related to the selected project within given timeframe.
3. Communicate technical information by means of oral as well as written Presentation skills in a professional manner.

Course Contents:

Project Stage – I Seminar is a partial work of the project including problem statement, literature review, project overview, implementation scheme and system design. Student should deliver a presentation on the selected project topic and submit a project stage I seminar report in standard format, certified by concerned authority.

Readings:

1. Journal Publications
2. Conference / Seminar Proceedings
3. Handbooks / Research Digests
4. Research articles on internet

Pedagogy:

1. Power Point Presentation
2. Videos
3. Group Discussion

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COURSE STRUCTURE

Course Code	**ECV621**			
Course Category	**Core Engineering**			
Course Title	**Web-based Open source**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**2**	**0**	**0**	**1+0+0**

The students can choose a online/MOOC/research based course of their choice. The level of course should be equivalent to University level course.

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COURSE STRUCTURE

Course Code	**ECV622**			
Course Category	**Core Engineering**			
Course Title	**Project Stage II Seminar**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**0**	**0**	**18**	**0+0+9**

Course Objectives:

1. To analyses, synthesize and conceptualize the identified problem
2. To conduct independent research to formulate and solve the chosen problem
3. Identify the modern tools required for the implementation of the project.
4. To communicate clearly, write effective reports and make effective presentations following the professional code of conduct

Course Outcomes:

After completion of this course students will be able to

1. Design and analyses a prototype for the identified problem during Stage I
2. Implement or develop the identified problem
3. Use modern tools for the implementation of the project.
4. Communicate technical information by means of oral as well as written presentation Skills in a professional manner.

Course Contents:

Project Stage – II Seminar is a partial work of the project including the fabrication/assembly of set up required for the project and experimentation. Student should publish paper on their project topic in reputed international journals/conferences. Student should deliver a presentation on the selected project topic, its implementation and submit a project stage II seminar report in standard format, certified by concerned authority.

Readings:

1. Journal Publications
2. Conference / Seminar Proceedings
3. Handbooks / Research Digests
4. Research articles on internet

Pedagogy:

1. Power Point Presentation
2. Videos
3. Group Discussion

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COURSE STRUCTURE

Course Code	**ECV631**			
Course Category	**Core Engineering**			
Course Title	**Web-based Open source**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**2**	**0**	**0**	**1+0+0**

The students can choose a online/MOOC/research based course of their choice. The level of course should be equivalent to University level course.

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COURSE STRUCTURE

Course Code	**ECV632**			
Course Category	**Core Engineering**			
Course Title	**Project Stage III Seminar**			
Teaching Scheme and Credits	**L**	**T**	**Laboratory**	**Credits**
Weekly load hrs	**0**	**0**	**18**	**0+0+9**

Course Objectives:

1. To carry out experimentation and testing of the project prototype
2. To write and present technical papers/articles in a professional manner.

Course Outcomes:

After completion of this course students will be able to

1. Analyze the results and draw conclusions
2. Publish and present technical papers/articles in a professional manner.

Course Contents:

In Project Stage – III, the student should complete the remaining part of the project with results and validation of results and conclusions. Student should publish paper on their project topic in reputed international journals/conferences. Student should deliver a presentation and demonstration on the selected project topic and submit a final project report in standard format, certified by concerned authority.

Readings:

1. Journal Publications
2. Conference / Seminar Proceedings
3. Handbooks / Research Digests
4. Research articles on internet

Pedagogy:

1. Power Point Presentation
2. Videos
3. Group Discussion

Checked By	**Checked By**	**Approved By**
(Prof. S.B.Somani) Coordinator	(Prof. Dr. V.V.Shete)	Dr. Arti. Khaparde Head of School ECE, MITWPU, Pune

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